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WHAT IS CLAIMED IS:

1. A fabrication process for a semiconductor integrated circuit device comprising:

- 5 (a) providing a semiconductor substrate;
- (b) forming a gate insulator film on a main surface of the semiconductor substrate;
- (c) forming a conducting film at least containing a metal film or a metal compound film on the gate insulator film;
- 10 (d) patterning the conducting film thereby forming a gate electrode;
- (e) nitriding or carbonizing a side wall for the gate electrode at a temperature of 600°C or lower; and
- (f) oxidizing the main surface of the semiconductor
- 15 substrate.

2. A fabrication process according to claim 1, wherein the side wall for the gate electrode is nitrided or carbonized at a temperature in the range of about 200°C to
20 500°C.

3. A fabrication process according to claim 1, wherein a plasma treatment using a nitrogen-containing gas is used for nitriding, thereby nitriding the side wall for the
25 gate electrode.

4. A fabrication process according to claim 1, wherein
a plasma treatment or a heat treatment using a
5 carbon-containing gas is used for carbonizing , thereby
carbonizing the side wall for the gate electrode.

5. A fabrication process according to claim 1, wherein
the main surface of the semiconductor substrate is
10 oxidized by plasma processing using an oxygen-containing
gas when oxidizing the main surface of the semiconductor
substrate.

15 6. A fabrication process according to claim 1, wherein
the main surface of the semiconductor substrate is oxidized
at a temperature of 600°C or lower.

7. A fabrication process according to claim 1, wherein
20 the main surface of the semiconductor substrate is oxidized
at a temperature in the range of about 200°C to 500°C.

8. A fabrication process according to claim 1, further
comprising:

restoring damages in the gate insulator film near the end of the gate electrode caused by patterning by oxidizing the main surface to restore the gate insulator film.

5 9. A fabrication process for a semiconductor integrated circuit device comprising:

- (a) providing a semiconductor substrate;
- (b) forming a gate insulator film on a main surface of the semiconductor substrate;
- 10 (c) forming a conducting film at least containing a metal film or a metal compound film on the gate insulator film;
- (d) patterning the conducting film thereby forming a gate electrode;
- (e) nitriding or carbonizing a side wall for the gate
- 15 electrode at a temperature of 600°C or lower;
- (f) oxidizing the main surface of the semiconductor substrate; and

further comprising including a step (d1) of adhering silicon or silicon compound on the side wall for the gate

20 electrode by a plasma processing using a silicon-containing gas after patterning the conducting film thereby forming a gate electrode before nitriding or carbonizing the side wall.

25 10. The fabrication process according to claim 9, wherein

silicon or silicon compound is adhered on the side wall for the gate electrode by a plasma processing using a silicon halide gas or a silicon hydride gas in the step (d1).

5 11. A fabrication process according to claim 1, wherein the gate electrode is made by;

providing a stacking structure comprising providing a polycrystalline silicon film,

providing a metal nitride film on the polycrystalline
10 silicon film, and

providing a metal film on the metal nitride film.

12. A fabrication process according to claim 11, wherein the metal nitride film comprises a nitride from the group

15 consisting of tungsten, molybdenum, tantalum or titanium, and the metal film comprises a metal film from the group consisting of tungsten, molybdenum, tantalum or titanium.

13. A fabrication process according to claim 11, wherein
20 the gate electrode further comprises a metal silicide film between the polycrystalline silicon film and the metal nitride film.

14. A fabrication process according to claim 13, wherein
25 the metal silicide film comprises a silicide from the group

consisting of tungsten, molybdenum, tantalum, titanium,
zirconium or hafnium.

15. A fabrication process according to claim 1, further
5 comprising:

providing the gate electrode with a stacked structure
comprising:

providing a polycrystalline silicon film;

providing a metal carbide film on the polycrystalline
10 silicon film;

and providing a metal film on the metal nitride film.

16. A fabrication process according to claim 1, further
comprising:

15 providing the gate electrode with a single layered
structure of a metal film.

17. A fabrication process according to claim 1, further
comprising:

20 providing the gate electrode with a stacked structure
comprising a polycrystalline silicon film and a metal
silicide film on the polycrystalline silicon film..

18. A fabrication process for a semiconductor integrated
25 circuit device comprising:

- (a) providing a semiconductor substrate;
- (b) forming a gate insulator film on a main surface of the semiconductor substrate;
- (c) forming a conducting film at least containing a metal
- 5 film or a metal compound film on the gate insulator film;
- (d) patterning the conducting film thereby forming a gate electrode;
- (e) nitriding or carbonizing a side wall for the gate electrode at a temperature of 600°C or lower; and
- 10 (f) oxidizing the main surface of the semiconductor substrate;

and further comprising forming a first insulator film on the conducting film after forming the conducting film and before patterning the conducting film thereby forming a gate

15 electrode, so that the first insulator film remains on the gate electrode and only the side wall of the gate electrode is exposed when nitriding or carbonizing the side wall for the gate electrode at a temperature of 600°C or lower.

- 20 19. A fabrication process according to claim 1, further comprising:

providing a plasma treatment by applying a nitrogen oxide gas or a carbon oxide gas before nitriding or carbonizing the side wall for the gate electrode at a

25 temperature of 600°C or lower; and

providing a nitrogen oxide gas or a carbon oxide gas
having a reducing property.

20. A fabrication process according to claim 1, further
5 comprising:

providing at least a portion of the gate insulator
film situated below a portion of the conducting film to be
removed when patterning the conducting film thereby forming
a gate electrode.

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